~~Specification~~

~~Control Loop for Digital Signals~~CONTROL LOOP FOR DIGITAL SIGNALS

BACKGROUND OF THE INVENTION

This invention relates to a control loop in which an input signal is converted, by multiplication by an integrator value, to an output signal that exhibits on average a constant reference value.

Such control loops are used, for example, as so-called AGC (automatic gain control) circuits for the automatic gain adaptation of digital signals. In automatic gain control, from an input signal, an output signal having a constant time-average value, whose level is as a rule adjustable and independent of the level of the input signal, is generated.

In detector circuits for high-frequency signals, the AGC is used to furnish, for further signal processing, an intermediate signal whose time-average level is constant, independently of the field strength of the detected signal of the input stage.

A known control loop for digital signals is illustrated in Figure 1. The energy of an output signal OUT exhibits on average a constant value that can be set via a reference value REF. High-energy input signals thus must be diminished in amplitude and low-energy input signals must be augmented in amplitude.

The output signal OUT is first adapted in a signal converter 1 in such a fashion that it can be compared to the reference value REF. If the output signal OUT is, for example, an electric current, then a voltage proportional to the current is derived to the signal converter and then compared to a reference voltage. Signal converter 1 can also adapt the output signal OUT in such

a fashion that the control behavior of the control loop is as favorable as possible. Signal-processing functions such as for example magnitude formation, squaring, or calculation of the distortion factor are suitable for this purpose. If one of the cited signal-processing functions is selected, it is guaranteed that only positive values are employed for the comparison even in case of a negative output signal OUT.

The comparison itself includes taking a difference with a difference element 2, in which the adapted output signal OUT is subtracted from the reference value REF. The difference element 2 supplies a difference ΔIN. The difference ΔIN is fed to an integrator element 3, which determines an integrator value IW therefrom. Integrator element 3 cumulates the difference ΔIN. If the difference ΔIN is positive, the integrator value IW is increased; if the difference ΔIN is negative, it is decreased. In a multiplication element 4, the input signal IN is multiplied by the integrator value IW. The result of this multiplication is the output signal OUT.

The circuit of FIG. ~~Figure~~ 1 can be described mathematically by

$\Delta IN = REF - IN * IW.$

In the steady-state condition, that is, when the control loop has built up to a steady state, $\Delta IN = 0$. Hence it follows that

$\Delta IN = REF - IN * IW = 0$ or, after manipulation,

$IW = REF/IN.$

Hence, finally, one obtains the desired output value OUT as

$OUT = IN * IW = IN * REF/IN = REF.$

The disadvantage of this circuit is the long buildup time that is required if the energy of the input signal IN deviates substantially from the reference value REF. In case of a large

deviation, several hundred cycles are required to set the reference value REF exactly. This long buildup time is not acceptable in time-critical control tasks.

It is a goal of the present invention to identify a control loop for the conversion of an input signal, by multiplication by an integrator value, into an output signal that exhibits on average a constant reference value, which control loop exhibits improved control behavior as a consequence of a simple supplementary circuit. ~~This goal is achieved with a control loop having the features of Claim 1. This goal is also achieved with a control loop having the features of Claim 4.~~

SUMMARY OF THE INVENTION

The invention has the advantage that the control behavior of the known control loop can be improved substantially with only a minor supplementary circuit. The individual components of the known control loop can continue to be used.

It is especially advantageous that the multiplication units and the division element can be implemented with simple shift registers (barrel shifters) if the constant factor or the reference value can be represented as a power of 2.

~~Advantageous further embodiments are characterized in dependent claims.~~

~~In what follows, the invention is explained in more detail on the basis of exemplary embodiments illustrated in the figures of the drawing. Corresponding elements are identified by the same reference numerals. The figures show:~~

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.~~igure~~ 1~~:~~ illustrates a known control loop;

FIG.~~igure~~ 2~~:~~ illustrates a control loop according to the invention having additional feedback; and

FIG.~~igure~~ 3~~:~~ illustrates a control loop according to the invention with counter.

DETAILED DESCRIPTION OF THE INVENTION

According to a first exemplary embodiment according to FIG.~~igure~~ 2, a difference element 2 has its output connected to a first multiplication element 5. Difference element 2 exhibits inputs for a reference value REF and an output signal OUT. Before it is fed to difference element 2, the output signal OUT can be adapted by a signal converter 1 to the reference value REF with respect to the physical unit. Difference element 2 forms the difference from the reference signal REF and the output signal OUT and passes this on to first multiplication element 5. This multiplies the difference ΔIN by a weighting factor GF. The result is passed on to an integrator element 3. Integrator element 3 integrates the difference ΔIN weighted with the weighting factor GF. The result of this integration is forwarded by integrator element 3 to a second multiplication element 4 as the integrator value IW. In second multiplication element 4, an input signal IN is multiplied by the integrator value IW. The result of this multiplication of second multiplication element 4 represents the output signal OUT.

The weighting factor GF is derived from the integrator value IW and fed back via first multiplication element 5 to integrator element 3. Favorable control behavior results if the integrator value IW is not used directly as weighting factor GF. It is more favorable to divide the integrator value IW by the reference value REF and weight the difference ΔIN therewith. The weighting factor GF in this case is the quotient of the integrator value IW and the reference value

REF. A division element 6 is provided for the performance of this division IW/REF. A first input of division element 6 is connected to an output of integrator element 3 in order to feed the integrator value IW to division element 6. A second input of division element 6 is connected to an input of difference element 2. The reference value REF is fed to division element 6 via the second input. Additionally, a multiplication unit 7 can be provided between first multiplication element 5 and integrator element 3. The output signal OUT is subtracted from the reference value REF and weighted with the weighting factor GF, which is calculated from IW/REF. The weighted difference is multiplied by a constant factor K in multiplication unit 7. The control behavior can be further improved through a suitable choice of the constant factor K. Here it is advantageous if the constant factor K exhibits a value in the buildup phase of the control loop that is different from the value in the steady state. For small values of K (e.g., K = 0.1), integrator element 3 needs more time for the difference ΔIN to be integrated. A longer integration time is advantageous in case of an input signal IN having a high level of noise. In the ideal case in which the input signal exhibits no noise, K can be chosen equal to 1 in order to achieve rapid stabilization.

Division element 6 and multiplication unit 7 can be implemented especially simply with shift registers. A prerequisite for doing so in the case of the division element is that the reference value REF can be represented as a power of 2 and, in the case of the multiplication unit, that the constant factor K, can be represented as a power of 2. The multiplication of a binary number by 2 corresponds to a shift of the binary number one place to the left. Analogously, division of a binary number by 2 corresponds to a shift of the binary number one place to the right.

According to a second exemplary embodiment according to FIG.~~igure~~ 3, difference element 2 again has its output connected to integrator element 3. Difference element 2 subtracts

from the reference value REF the output signal OUT, which may be adapted in signal converter 1, and forwards the difference ΔIN to integrator element 3. In this exemplary embodiment, integrator element 3 can take on only values between a lower and an upper threshold. If the integrator value already lies near the upper threshold, subsequent integration takes place near the lower threshold. If the integrator value IW lies near the lower threshold, then in case of a further decrease below the lower threshold, counting continues near the upper threshold. Integrator element 3 thus exhibits an overflow and an underflow. Along with the integrator value IW, there is at a carry output UA a count signal, which passes on any passage beyond one of the thresholds to a counter 8. The counter increments its count in case of overflow and decrements the count in case of underflow. Counter 8 has its output connected to an input multiplication element 9. Input multiplication element 9 multiplies the input signal IN by the count, which represents the number of passages beyond the lower and upper threshold. The result of this multiplication is fed to second multiplication element 4, which multiplies it by the integrator value IW in order to obtain the output signal OUT.

With the exemplary embodiment according to FIG.~~igure~~ 3, the input signal IN is scaled with a scaling factor. The scaling factor is 2^n, where n corresponds to the count of counter 8. In case of large deviations of the input signal IN from the reference value REF, the scaling brings the input signal to the order of magnitude of the reference value. Thus it is guaranteed that the ratio of integrator value to reference value lies near 1.

A further improvement of the control behavior is achieved if an intermediate multiplication element 10 is provided between integrator element 3 and difference element 2. The difference ΔIN is weighted with this by the factor K.

Although the present invention has been illustrated and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: